

What is claimed is:

1. A multiplexer circuit comprising:
 - a first tri-state inverter circuit that is coupled to a first multiplexer input node, a first multiplexer output node, and a first switch node, wherein
 - the first tri-state inverter circuit is capable of a high-impedance output at the first multiplexer output node;
 - a second tri-state inverter circuit that is coupled to a second multiplexer input node, a second multiplexer output node, and a second switch node, wherein
 - the second tri-state inverter circuit is capable of a high-impedance output at the second multiplexer output node;
 - a first switch circuit that is coupled between the first switch node and the second multiplexer output node; and
 - a second switch circuit that is coupled between the second switch node and the first multiplexer output node.
2. The multiplexer circuit of Claim 1, wherein
 - the first tri-state inverter circuit is configured to isolate the first multiplexer input node from the first multiplexer output node if a control signal corresponds to a second logic level.
3. The multiplexer circuit of Claim 2, wherein
 - the second tri-state inverter circuit is configured to isolate the second multiplexer input node from the second multiplexer output node if a control signal corresponds to the second logic level,
 - the first switch circuit is configured to:
 - short the first switch node to the second output node if the control signal corresponds to a second logic level, and
 - isolate the first switch node from the second output node if the control signal corresponds to a first logic level, and

13. The multiplexing column driver circuit of Claim 11, wherein
the selected pair further comprises:
a high-range decoder circuit that is coupled between a first decoder node and a third multiplexer input node; and
a low-range decoder circuit that is coupled between a second decoder node and a fourth multiplexer input node.
14. The multiplexing column driver circuit of Claim 13, wherein
the selected pair further comprises:
a second two-by-two multiplexer circuit that is coupled to the third multiplexer input node, the fourth multiplexer input node, a third multiplexer output node, and a fourth multiplexer output node.
15. The multiplexing column driver circuit of Claim 11, wherein
the first tri-state inverter circuit is configured to isolate the first multiplexer input node from the first multiplexer output node if a control signal corresponds to a second logic level.
16. The multiplexing column driver circuit of Claim 14, wherein
the second tri-state inverter circuit is configured to isolate the second multiplexer input node from the second multiplexer output node if a control signal corresponds to the second logic level,
the first switch circuit is configured to:
short the first switch node to the second output node if the control signal corresponds to the second logic level; and
isolate the first switch node from the second output node if the control signal corresponds to a first logic level; and
the second switch circuit is configured to:
short the second switch node to the first multiplexer output node if the control signal corresponds to the second logic level; and

isolate the second switch node from the first multiplexer output node if the control signal corresponds to the first logic level.

17. The multiplexing column driver circuit of Claim 11, wherein the first tri-state inverter circuit is further configured:
 - to provide an inverter output signal at the first multiplexer output node in response to a first multiplexer input signal if the control signal corresponds to a first logic level, and
 - provide the inverter output signal at the first switch node in response to the first multiplexer input signal.
18. The multiplexing column driver circuit of Claim 11, wherein the first two-by-two multiplexer circuit consists of twelve transistors; the first tri-state inverter circuit is configured to receive a first multiplexer input signal;
 - the second tri-state inverter circuit is configured to receive a second multiplexer input signal; and
 - the first two-by-two multiplexer circuit is arranged such that
 - the first multiplexer input signal drives at most two transistors of the twelve transistors, and
 - the second multiplexer input signal drives at most another two transistors of the twelve transistors.
19. The multiplexing column driver circuit of Claim 11, wherein the first tri-state inverter circuit is configured to:
 - receive a first multiplexer input signal at the first multiplexer input node;
 - receive a first control signal;
 - receive a complement of the first control signal;
 - provide a first inverter signal at the first switch node and a fifth switch node in response to the first multiplexer input signal; and

the first means for providing is capable of a high-impedance output at the first multiplexer output node;

a second means for providing a second inverted signal at a second multiplexer output node in response to a second multiplexer input signal if the control signal corresponds to the first logic level, wherein

the second means for providing is capable of a high-impedance output at the second multiplexer output node; and

a means for coupling the first inverted signal from a first switch node to the second multiplexer output node if the control signal corresponds to a second logic level.